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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/777,560	02/11/2004	Harry S. Luan	108-18.1	5757

7590 04/05/2006

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EXAMINER	
NGUYEN, THINH T	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 04/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/777,560	LUAN ET AL.	
	Examiner	Art Unit	
	Thinh T. Nguyen	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11/2/05, 1/18/06*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14 and 22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/2/2005*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED OFFICE ACTION

1. Applicant 's election of claims 1-14,22 for prosecution of the application without traverse in the communication with the Office on 1/18/2006 is acknowledged.

2. In response to applicants' communications on 11/1/2005 and 1/18/2000 , the Official Office Action Issued on 7/26/2005 is withdrawn.

3. Claims 1-14,22 are currently pending in the Application.

Specification

4. The specification has been checked to the extent necessary to determine the presence of all possible minor errors. However, the applicant cooperation is requested in correcting any errors of which the applicant may become aware in the specification.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(b) that form the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claim 1,6, are rejected under 35 U.S.C. 102(b) as being anticipated by Gallagher et al. (U.S. Patent 5,640,343) .

REGARDING CLAIM 1

Gallagher discloses (fig 1A,Fig 2) an integrated circuit comprising: a first array of memory cells, each memory cell in the first array comprising a resistive element (column 2 lines 33-34) and a Schottky diode (column 10 line 61-64) coupled in series and having first and second terminals; a first plurality of bit lines, one bit line for each column of the first array, each bit line coupled to the first terminal of memory cells in a respective column of the first array; and a first plurality of word lines, one word line for each row of the first array, each word line coupled to the second terminal of memory cells in a respective row of the first array.

REGARDING CLAIM 6

Gallagher discloses (fig 1A,Fig 2) a memory arrays with cells that are formed at cross-point between a bit line and a word line.

7. Claim 1, 6, 7 ,11 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson et al. (US patent 6,185,122)

REGARDING CLAIM 1

Johnson discloses (fig 4(a),fig 4(b),fig 8(b)) an integrated circuit comprising: a first array of memory cells, each memory cell in the first array comprising a resistive element (column 9 line 44-49) and a Schottky diode (column 8 line 1) coupled in series and having first and second terminals; a first plurality of bit lines (fig 4(b) refrence21) , one bit line for each column of the first array, each bit line coupled to the first terminal of memory cells in a

respective column of the first array; and a first plurality of word lines (fig 4(b) reference 20) , one word line for each row of the first array, each word line coupled to the second terminal of memory cells in a respective row of the first array.

REGARDING CLAIM 6

Johnson discloses (fig 4(a),fig 4(b),fig 8(b)) a memory arrays with cells that are formed at cross-point between a bit line and a word line.

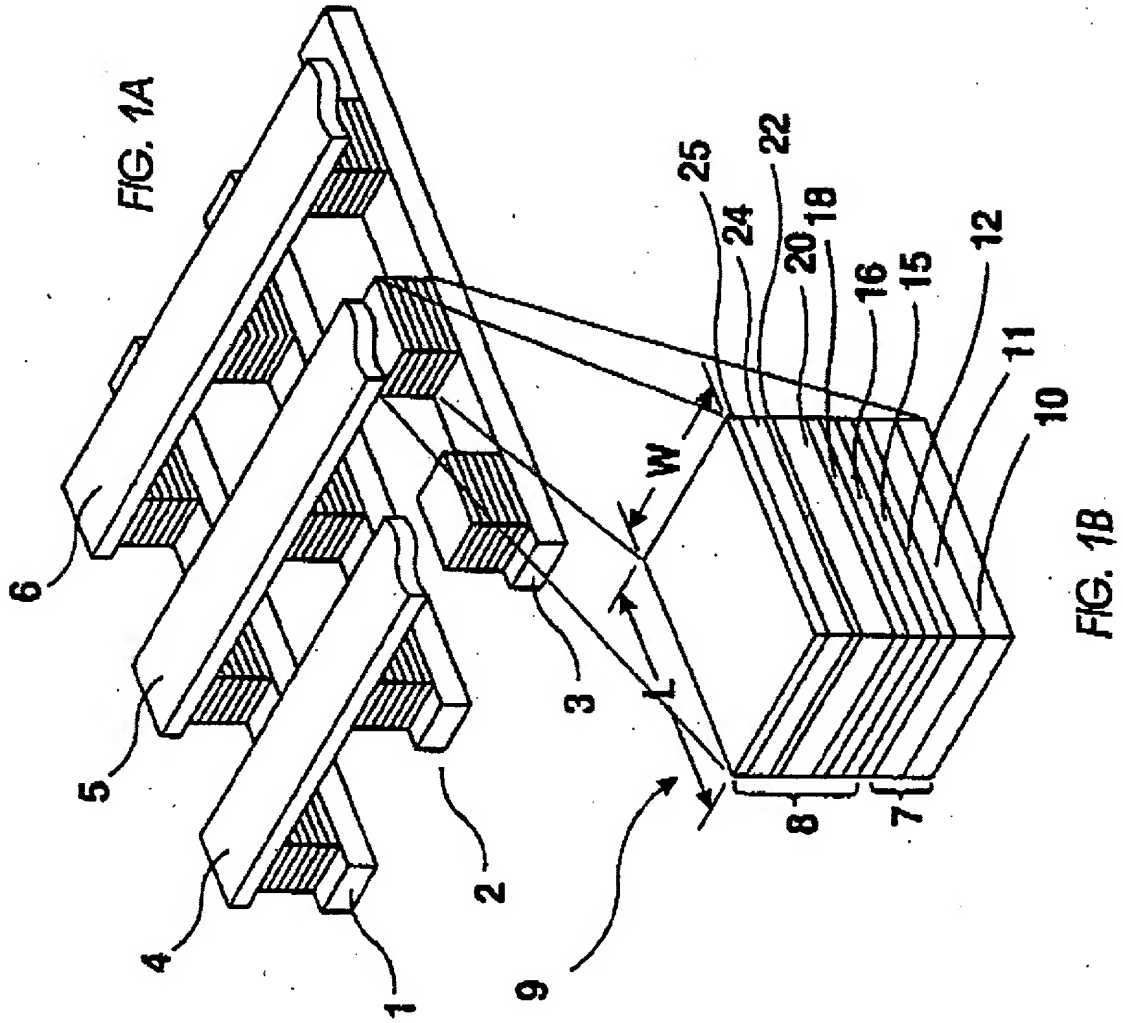
REGARDING CLAIM 7

Johnson discloses (fig 4(a),fig 4(b),fig 8(b) ,column 10 line 5-10) a memory that can be program and that has two states.

REGARDING CLAIM 11

Johnson discloses (fig 4(a),fig 4(b),fig 8(b) , fig 5) an integrated circuit comprising: a second array of memory cells, each memory cell in the second array comprising a resistive element and a Schottky diode coupled in series and having first and second terminals; a second plurality of bit lines, one bit line for each column of the second array, each bit line coupled to the first terminal of memory cells in a respective column of the second array; and

a second plurality of word lines, one word line for each row of the second array, each word line coupled to the second terminal of memory cells in a respective row of the second array.



Gallagher REFERENCE

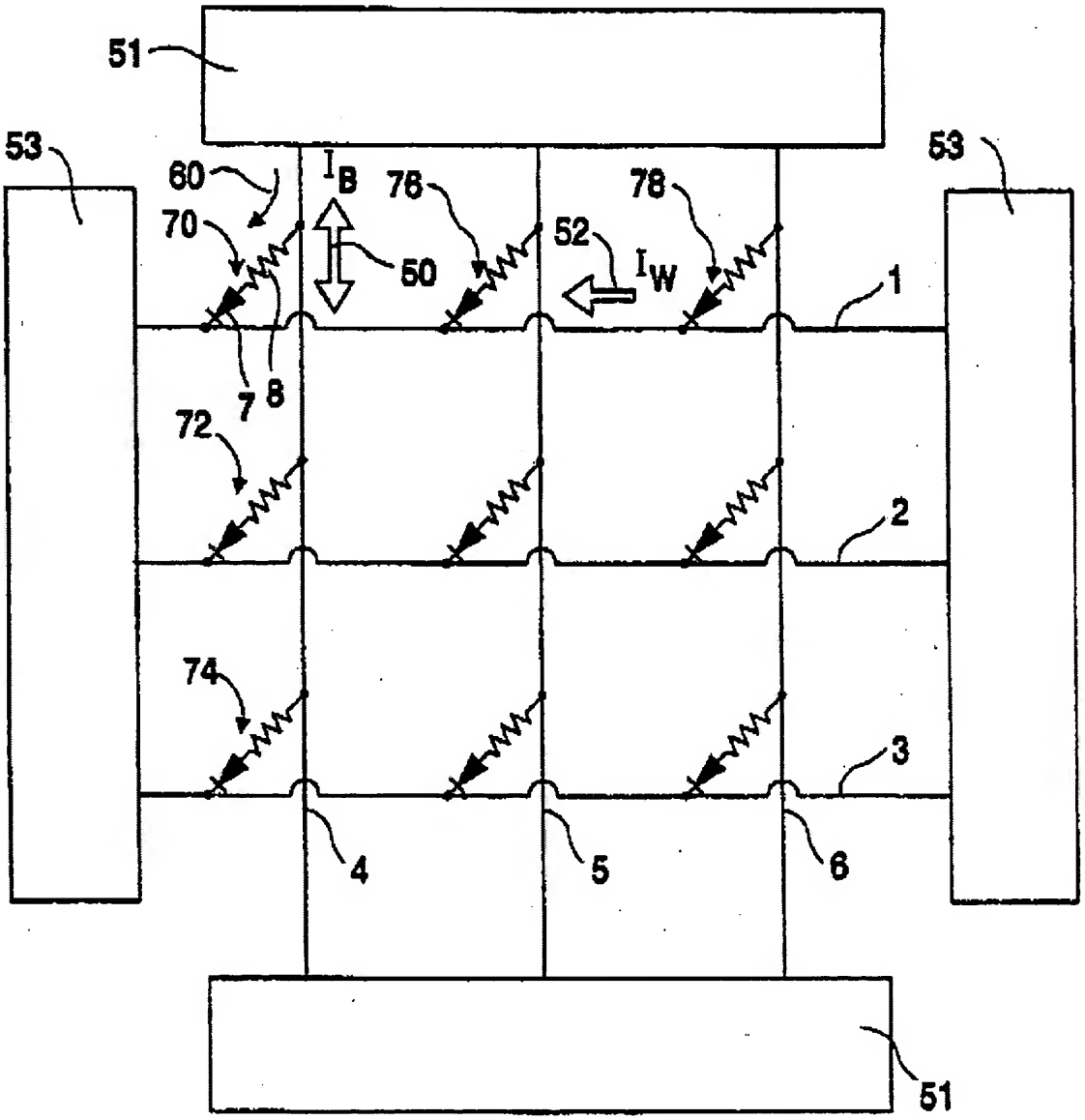


FIG. 2

Gallagher REFERENCE

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102(e) that form the basis for the rejections under this section made in this office action.

A person shall be entitled to a patent unless --

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claim 1,6 are rejected under 35 U.S.C. 102(e) as being anticipated by Kim (U.S. Patent 6,750,540) .

REGARDING CLAIM 1

Kim discloses (fig 2,column 3 lines 31-32,claim 1) an integrated circuit comprising: a first array of memory cells, each memory cell in the first array comprising a resistive element (column 6 line 1-5) and a Schottky diode (column 3 line 40,claim 1) coupled in series and having first and second terminals; a first plurality of bit lines, one bit line for each column of the first array, each bit line coupled to the first terminal of memory cells in a respective column of the first array; and a first plurality of word lines, one word line for each row of the first array, each word line coupled to the second terminal of memory cells in a respective row of the first array.

REGARDING CLAIM 6

Kim discloses (claim 1, Fig 2) a memory arrays with cells that are formed at cross-point between a bit line and a word line.

Claim Rejections - 35 USC § 103

10. The following is a quotation of U.S.C. 103(a) which form the basis for all obviousness rejections set forth in this office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.
> Patentability shall not be negatived by the manner in which the invention was made.

11. Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gallagher et al. (U.S. Patent 5,640,343) in view of Shanks (US patent 4,203,123).

REGARDING CLAIM 5

Gallager discloses (fig 1A,Fig 2) all the invention including a schottky switching element except for the specific detail that the schottky diode are made of amorphous silicon. Shank , however, (in fig 3 in column 4 lines 5-11) discloses a memory device that use thin film amorphous silicon . It would have been obvious to one of ordinary skill at the time the invention was made to incorporate the amorphous silicon thin film schottky diode disclosed by Shank in the Gallager device since both Shank and Gallagher are in the same field of endeavor of making semiconductor memory device that have memory element and switching element connected in serie.

12. Claims 2,3 ,4, are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US patent 6,750,540) in view of Rinerson (U.S. patent 6,870,755)

REGARDING CLAIM 2,3

With regard to claim 2 and 3, as discussed in the rejection of claim 1, Kim disclosed All the invention including a schottky diode and a CMR (Colossal Magnetic Resistor) resistive element except for the specific that the CMR is a perovskite PCMO (Pr07Ca0.3MnO3) resistive material.

Rinerson (the abstract, fig 2, fig 5,column 5 line 27-45) discloses a integrated memory circuit using a perovskite PCMO (Pr07Ca0.3MnO3) resistive material.

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporate perovskite PCMO (Pr07Ca0.3MnO3) resistive material as disclosed by Rinerson in the Kim device since both Kim and Rinerson are in the same endeavor of fabricating cross point memory device with resistive element and steering or isolation device.

REGARDING CLAIM 4

Rinerson (column 4 lines 25-32,column 5 lines 27-45) discloses the use of Perovskite Colossal resistive material.

The rationale as why claim 4 is Obvious over Kim in view of Rinerson has been discussed in the rejection of claim 2,3

13. Claims 8,9 ,10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kim (US patent 6,750,540) in view of Rinerson (US patent 6,870,755) and in further view by Marquot et al. (US patent 5,978,262)

REGARDING CLAIM 8

As discussed in the rejection of claim 2,3 the combined teachings by Kim and Rinerson disclose all the invention except for the use of bit line driver that can read and program the memory cell. Marquot; however, teaches (in the abstract) the use of bit line driver that can read and program the Matrix non-volatile magnetic memory cell.

It would have been obvious to one of ordinary skill in the art the time the invention was made to incorporated the bit line driver that can read and program the Matrix non-volatile magnetic memory cell invented by Marquot in the Device invented by Kim in view of Rinerson.

The rationale is as the following: as person skilled in the art at the time the invention was made would have been motivated to reduce the overall programming time for the Kim in view of Rinerson as suggested by Marquot (see Marquot reference column 2 lines 9-10).

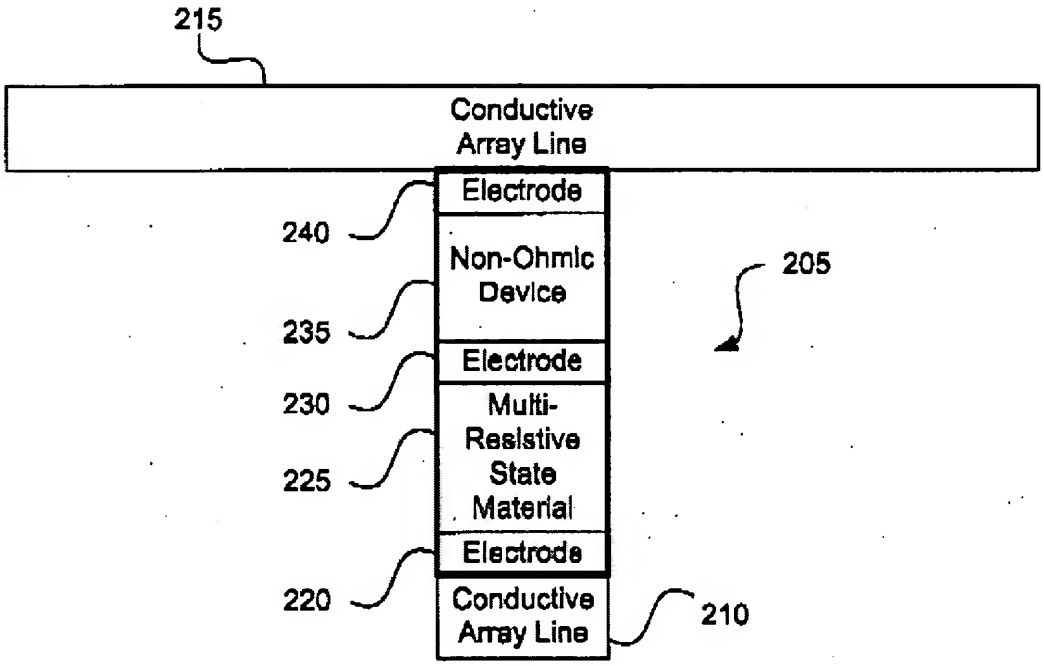

215
Conductive Array Line
Electrode
240
Non-Ohmic Device
205
235
Electrode
230
Multi-Resistive State Material
225
Electrode
220
Conductive Array Line
210

FIG. 2

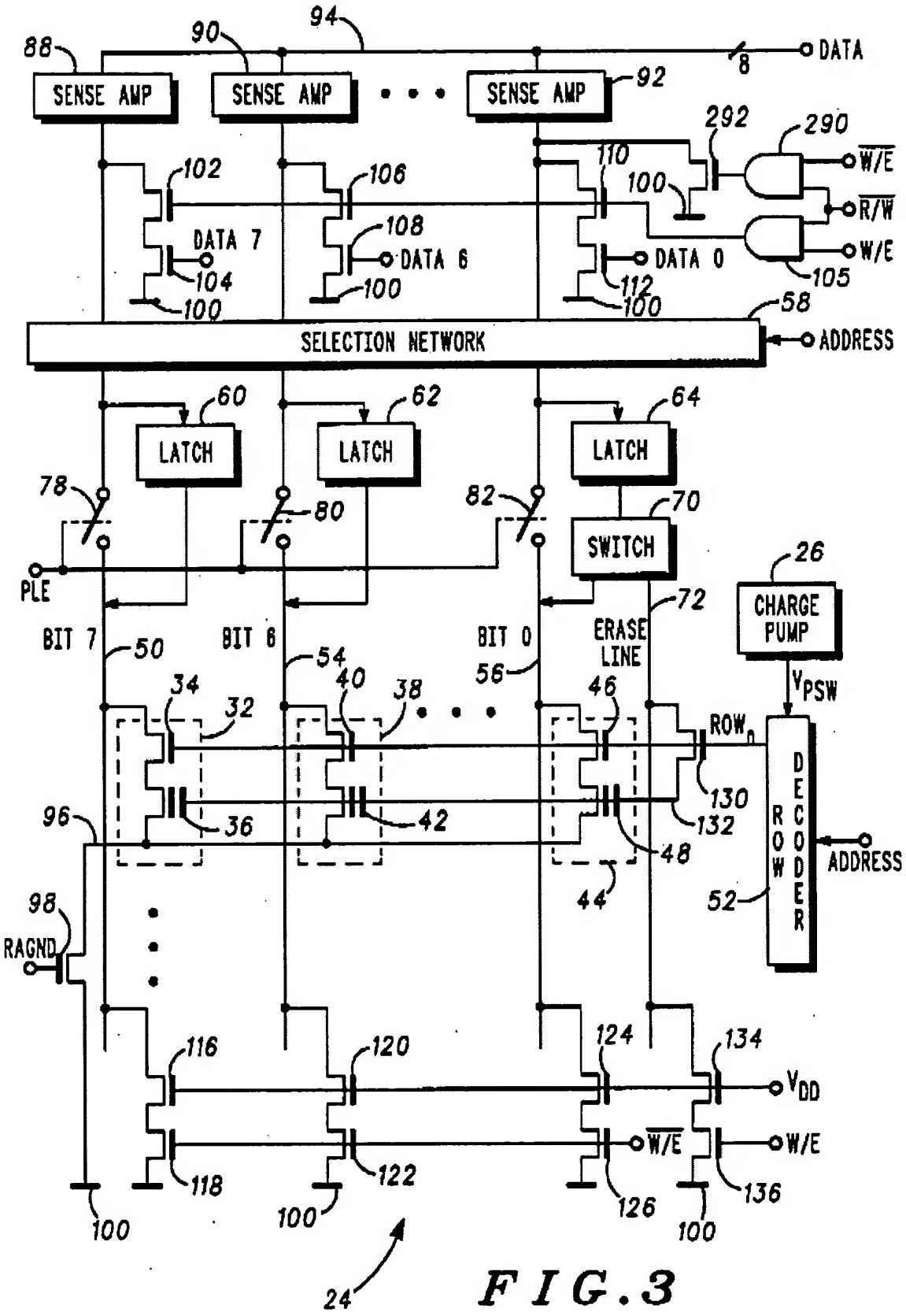

SENSE AMP
SENSE AMP
SENSE AMP
DATA
8
88
90
94
92
292
290
W/E
R/W
W/E
105
110
100
102
106
108
DATA 7
DATA 6
DATA 0
104
112
SELECTION NETWORK
58
ADDRESS
60
62
64
LATCH
LATCH
LATCH
78
80
82
70
SWITCH
PLE
26
CHARGE PUMP
72
ERASE LINE
BIT 7
BIT 6
BIT 0
50
54
56
34
32
40
38
46
V_{PSW}
ROW_n
96
36
42
130
132
48
44
ROW DECODER
52
ADDRESS
98
RAGND
116
120
124
134
V_{DD}
$\overline{W/E}$
W/E
118
122
126
136
24

FIG. 3

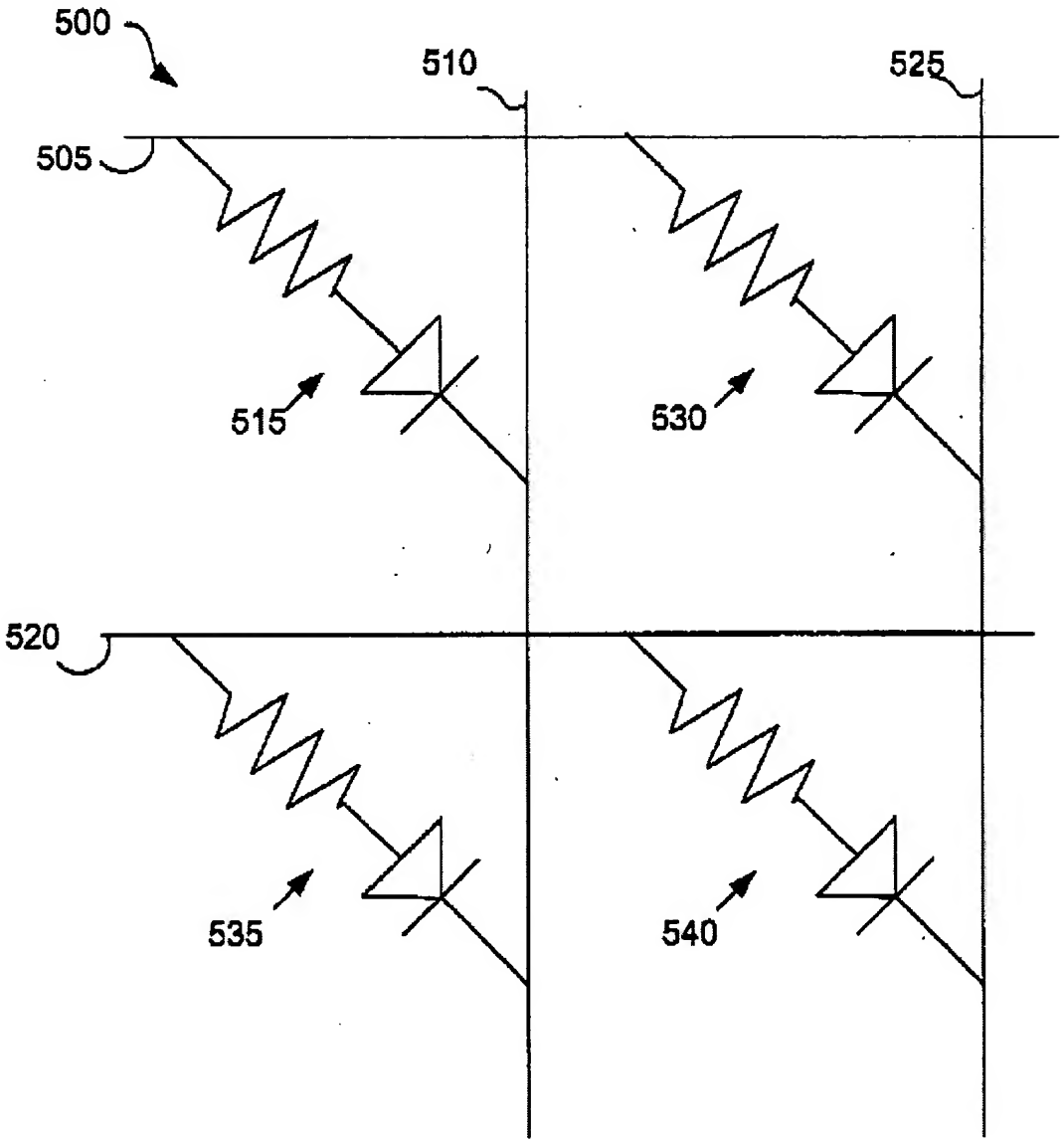


FIG. 5

REGARDING CLAIM 9

Marquot discloses (in fig 3,column 3 lines 42-50) a word line decoder (Marquot called it the row decoder) for reading and programming the memory cell. Noted that on top of the row

decoder in fig 2 there is a charge pump 26 that can be used among other thing to program the memory cells.

The rationales why claim 9 is obvious over prior arts have been set forth in the rejection of claim 8.

REGARDING CLAIM 10

Marquot discloses (in fig 3) disclose a plurality of sense amplifiers (reference 88,90,92) Those are coupled to the bit lines to read the state of the memory cells.

The rationales why claim 10 is obvious over prior arts have been set forth in the rejection of claim 8.

14. Claim 12,13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al (US patent 6,185,122) in view of Marquot et al. (US patent 5,978,262)

REGARDING CLAIM 12

With regard to claim 12 , as discussed in the rejection of claim 1, Johnson (fig 4(a),fig 4(b),fig 8(b) ,fig 10(a),fig 10 (b) ,fig 11) discloses all the invention except for going into detail about the use of decoder and sense amplifiers. Marquot (in fig 3,column 3 lines 42-50) discloses a word line decoder (Marquot called it the row decoder) and a plurality of sense amplifiers

It would have been obvious to one of ordinary skill in the art to incorporated word line decoders and a plurality of sense amplifiers invented by Marquot in the Johnson device.

The rationale is as the following: as person skilled in the art at the time the invention was made would have been motivated to reduce the overall programming time for the Johnson device as suggested by Marquot (see Marquot reference column 2 lines 9-10).

REGARDING CLAIM 13

Rinerson discloses (in column 6 lines 39-40) the use of a perovsksite film.

The rationales why claim 13 is obvious over Johnson in view of Marquot have been discussed in the rejection of claim 12..

15. Claim 14 rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al (US patent 6,185,122) in view of Marquot et al. (US patent 5,978,262) and in further view by Shanks (US patent 4,203,123)

With regard to claim 14 , as discussed in the rejection of claim 12, Johnson in view of Marquot disclose all the invention except for the use of thin film amorphous silicon schottky diode.

Shank , however, (in fig 3 in column 4 lines 5-11) discloses a memory device that use thin film amorphous silicon . It would have been obvious to one of ordinary skill at the time the invention was made to incorporate the amorphous silicon thin film schottky diode disclosed by Shank in the Johnson in view of Marquot device since Shank, Johnson and Marquot all are in the same field of endeavor of making matrix semiconductor memory device .

16. Claims 22 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson et al (US patent 6,185,122) in view of Smith et al. (US patent 6,625,055).

With regard to claim 22, as discussed in the rejection of claim 11 ,Johnson discloses all the invention except for an isolation layer between a first layer and a second layer, wherein the first layer is formed by the first array of memory cells. the first plurality of bit lines. and the

first plurality of word lines. and wherein the second layer is formed by the second array of memory cells. the second plurality of bit lines. and the second plurality of word lines.

Smith (,fig 3, fig 5) however, discloses a memory semiconductor device that have isolation layer (fig 5 reference 508) between a first layer and a second layer, wherein the first layer (fig 5 reference 502) is formed by the first array of memory cells. the first plurality of bit lines. and the first plurality of word lines (fig 5 reference 510, 512) . and wherein the second layer (fig 5 reference 504) is formed by the second array of memory cells. the second plurality of bit lines. and the second plurality of word lines.

It would have been obvious to one of ordinary skill in the art to incorporate isolation layer between a first layer and a second layer, wherein the first layer is formed by the first array of memory cells, the first plurality of bit lines, and the first plurality of word lines, and wherein the second layer is formed by the second array of memory cells. the second plurality of bit lines. and the second plurality of word lines in the Johnson device since both Smith and Johnson are in the same field of endeavor of making stacked matrix semiconductor memory device.

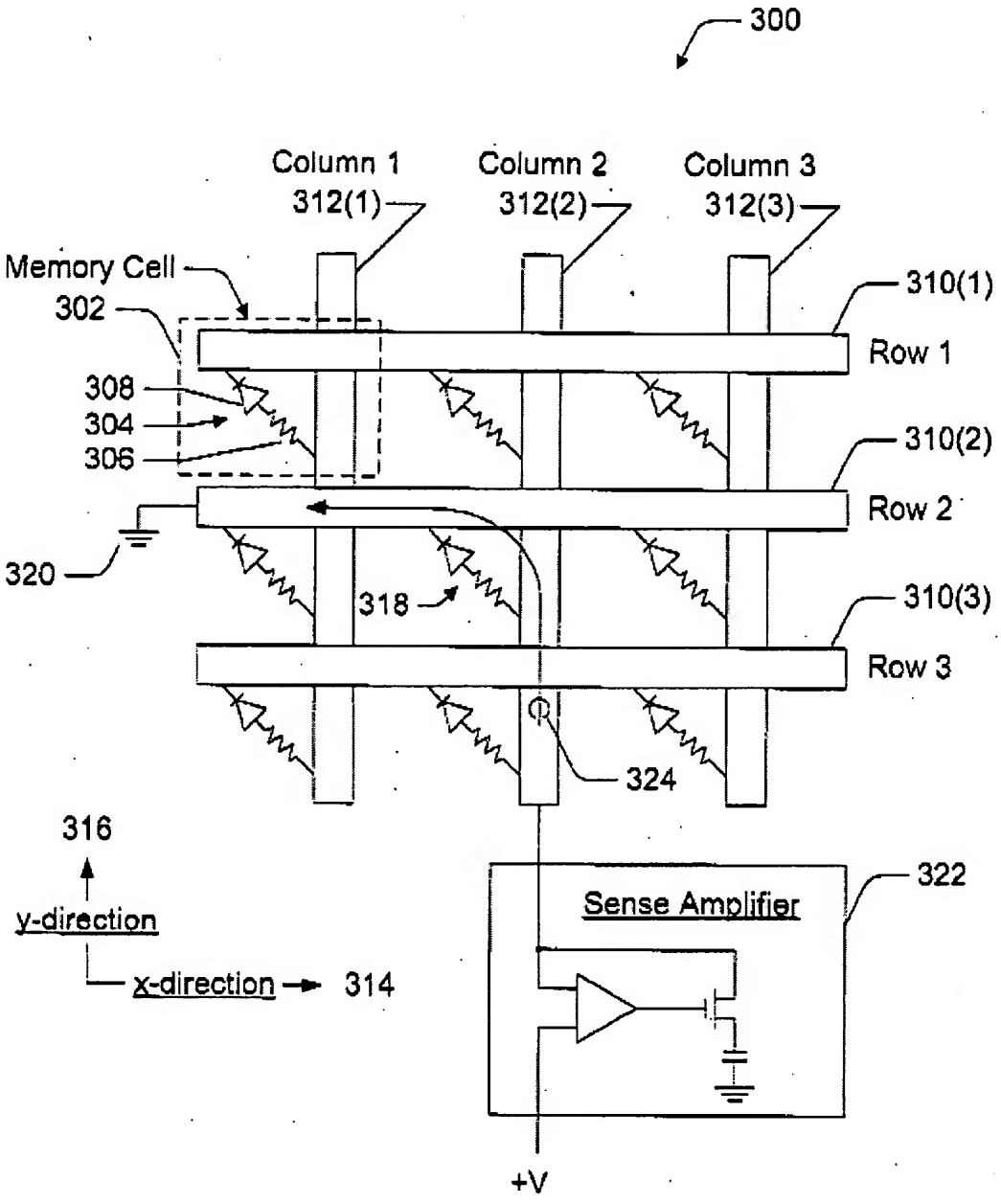

300
Column 1
312(1)
Column 2
312(2)
Column 3
312(3)
Memory Cell
302
310(1)
Row 1
308
304
306
310(2)
Row 2
320
318
310(3)
Row 3
324
316
y-direction
x-direction
314
322
Sense Amplifier
+V

Fig. 3

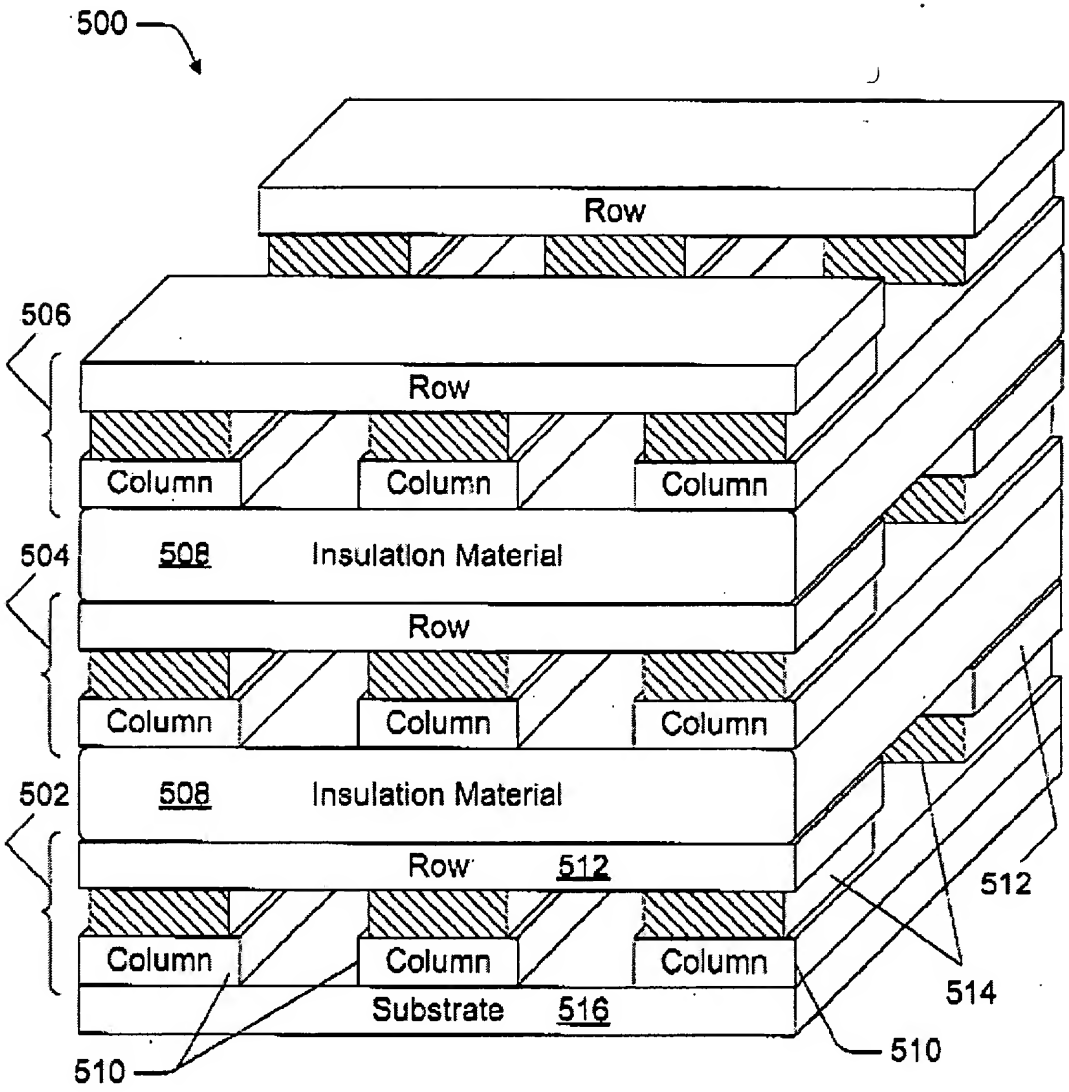


Fig. 5

JOHNSON REFERENCE

17. When responding to the office action, Applicants are advised to provide the examiner with the line numbers and the page numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

18. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the day of this letter. Failure to respond within the period for response will cause the application to be abandoned (see M.P.E.P. 710.02(b)).

CONCLUSION

19. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thinh T Nguyen whose telephone number is 571-272-1790. The examiner can normally be reached on Monday-Friday 9:00am-6:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached at 571-272-1787.

The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval [PAIR] system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thinh T. Nguyen TTN

Art Unit 2818

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Supervisory Patent Examiner
Technology Center 2800